

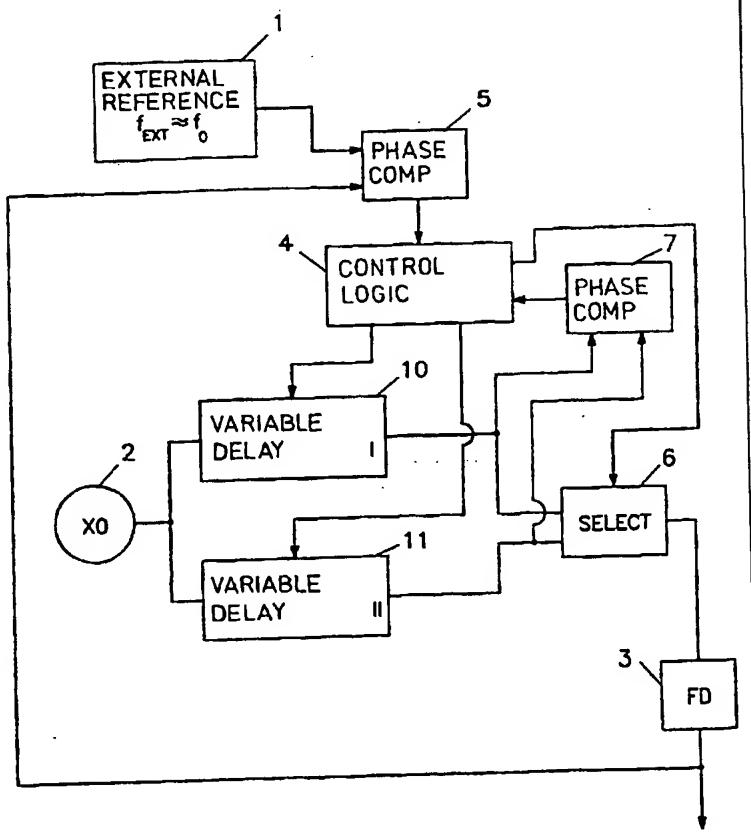
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(54) Title: DIGITAL CONTROLLED XTAL OSC			
(57) Abstract			
<p>According to the present invention, an unlimited number of steps or increments of given size are obtained in a delay line for phase alignment of, for instance, the signal from a crystal oscillator (XO) by momentarily switching between two parallel delay lines. One delay line operates as an active or enabled delay line while the other line is disabled or inactive. It is ensured at the same time that the inactive delay line produces a signal which has the same relative phase as the active delay line, this absolute phase differing by <math>N \times 2\pi</math>, where <math>N</math> is a positive or a negative integer other than zero. The inventive method and the inventive device enable the active delay line to operate constantly within its regulation range and the phase of the local oscillator can be kept continuously locked to the phase of the reference signal. The inventive device also includes an oscillator (2), a phase comparator (5) and counter logic (4) and a further phase comparator (7) and a selection circuit (6) for signal selection from that one of the two parallel delay lines (10, 11) that has been placed in its active mode.</p>			



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**DIGITAL CONTROLLED XTAL OSC****TECHNICAL FIELD**

The present invention relates to a method and to an arrangement for adding or subtracting an unlimited number of small delay steps or increments for the purpose of compensating for a phase difference and a frequency difference between a local clock and a reference clock, and more particularly to the use of a method and a device which use two delay lines in parallel.

**PRIOR ART**

Present-day conventional data-based electronic systems are all based essentially on the presence of a local clock generator whose clock frequency controls the local system. In order to be able to work with the local system in relation to the outer world, it is necessary generally to synchronize the local clock with the outer world. This is normally effected by phase locking the local oscillator to some external reference with the aid of a feedback phase locking loop. Such a device is normally designated PLL (Phase Locked Loop). In this regard, the local oscillator may be a freely oscillating oscillator or an oscillator which uses a crystal or similar type of resonator element as the frequency determining element. In this latter case, the oscillator retains frequency and phase with a high degree of accuracy and over a longer period of time, even should the external reference fail. There is normally used a phase detector which applies an analog control voltage to a voltage controlled oscillator (VCO) or a voltage controlled crystal oscillator (VXCO).

According to the present standpoint of techniques, it is possible to compensate for a delay which expresses itself as a phase error against the local clock with the aid of a variable delay line. For instance, the undesired external delay can be compensated for by virtue of the variable delay inserting a corresponding delay

in the clock generator of the local system, so as to equalize the phase error. There is also often selected a fixed additional delay together with the variable delay, thereby enabling the variable delay to be made smaller. However, this will not be successful when the delay to be compensated may be arbitrary and vary widely with time.

For instance, US-A 4,868,514 discloses an apparatus and a method for digital compensation of oscillator operation. This publication intends to provide phase alignment between two clock signals which operate at practically the same frequency, wherein a variable digital delay delivers a corrected clock signal whose phase is aligned with the phase of the other clock. US-A 5,079,519 discloses a digital phase locked loop for a logic gate group, wherein the arrangement maintains a determined phase delay between an input signal and an output signal by virtue of a counter selecting an appropriate tapping-point on a delay line. UK Patent Specification GB-A 2,236,223 discloses a similar digital phase locked loop, which also includes a tapped delay line which produces a multiple of signals of different phases, of which one signal is chosen through a selection circuit. Other examples of this technique using a delay line in accordance with the present standpoint of techniques are to be found in other documents, such as in US-A 5,012,198, US-A 4,795,985 and US-A 4,677,648, for instance.

The following advantages are obtained with the technique of choosing a digital solution instead of the conventional solution using a VCO:

- A digital solution can be integrated readily in a user specific integrated circuit (ASIC).
- Error monitoring mechanisms can be readily implemented in a digital system and added thereto. This is more difficult in the case of an analog solution, since it is then necessary to measure the analog control signal.

- A digital solution is also generally more construction-friendly and production-friendly than an analog solution.

A common drawback with all of the known prior art solutions is that problems occur when the delay is changed with time to an extent such that the delay lies in the proximity of the maximum or the minimum possible delay that can be obtained with the variable delay line. In those cases where large changes in the delay are expected, it is necessary to include in the delay line a large delay interval which will enable the locked phase alignment in the circuit to be readily maintained. In turn, such a large phase locking interval will result in relatively poor phase resolution and/or phase accuracy. Another method of overcoming this drawback is to include a logic circuit which will ensure that it is possible to jump back, for instance  $2\pi$  in absolute phase with the delay line and again lock-in the phase locking loop somewhere in the centre of the adjustable region of the delay line.

A backward jump of one period ( $2\pi$ ) in the delay is not trivial, since the step length can vary greatly in different examples of the same circuit and may, for instance, be in the order of 0.1-0.3 ns. In addition, a certain amount of time is needed to ensure that the relative phase coincides after the phase jump, and consequently noticeable discontinuities can be expected with necessity when practicing this technique.

There is therefore a need for a simple solution to the problem of causing an oscillator to faithfully follow the phase of an external or internal reference signal whose phase changes with time by many whole periods, but while retaining a continuous phase for the output signal from the oscillator without the occurrence of phase jumps or transients in the output signal.

#### SUMMARY OF THE INVENTION

In accordance with a method and a device according to the present invention, there is created a possibility of adding or subtract-

ing an unlimited number of small delay steps to and from a clock signal from an oscillator, there being used a delay line which has a limited number of series-connected small delay elements and the signal is tapped-off after a digitally selectable number of delay steps.

In accordance with a first object of the present invention, an unlimited number of steps of given size are obtained in a delay line by momentarily switching to another delay line, wherein this momentary switching between delay lines is effected by switching from an enabled or active delay line to an inactive or disabled phase-aligned delay line which has been regulated so that the inactive delay line has a delay which is suitably greater or smaller than the delay of the active delay line by one clock period, thereby enabling the phase of the stable local oscillator to be maintained continuously even when the phase of the reference signal continuously changes, for instance when there is constantly a small frequency difference between the frequency of the local oscillator and the frequency of the reference signal.

In accordance with a second object of the present invention, after having switched momentarily between delay lines, the delay line which was earlier active becomes passive and is prepared for the next momentary switching between said lines in a corresponding manner when the phase again changes to an extent which makes it suitable to again time-shift the delay line by, for instance, one clock period but while maintaining continuous locking of the oscillator output signal.

According to a first embodiment of the present invention, there is used a delay line array comprised of two separate delay lines having digitally selectable tapping points to achieve an active and a passive delay line for phase alignment of the signal from the oscillator.

According to a second embodiment of the present invention, the delay line array used is comprised of one delay line having two arrays of digitally selectable tapping points to obtain an active and a passive delay line for phase alignment of the signal from the oscillator.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described with reference to exemplifying embodiments thereof and also with reference to the accompanying drawings, in which

Figure 1 illustrates a conventional device for aligning the phase of a local clock, for instance a crystal oscillator, to an external reference;

Figure 2 illustrates a conventional device for aligning the phase of a local clock to an undesired internal delay;

Figure 3 illustrates a simplified device constructed in accordance with the present invention for continuously aligning a local oscillator with the aid of two alternating delay lines;

Figure 4 illustrates a simplified device according to the present invention for continuously aligning a local oscillator with the aid of a delay line having two mutually independent tapping points; and

Figure 5 is a block schematic illustrating an application which uses three oscillator arrays in accordance with the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

Figure 1 is a simplified block schematic which illustrates phase compensation of an internal oscillator in relation to an external reference signal which is also the subject of an external delay, in accordance with the known prior art. This example of the known

prior art assumes that the oscillator has, in principle, the same frequency as the reference, since the circuit solely compensates for phase errors. In the illustrated case, it will be necessary sooner or later to reset the variable delay with at least plus or minus one period, so as not to fall outside the regulation or adjustment range of the delay line.

Figure 2 is a block schematic which illustrates correspondingly the phase compensation of a local oscillator in accordance with the same principle as that illustrated in Figure 1. The undesired delay occurs, for instance, because clock control normally requires buffering in order to be able to provide all digital circuits on a card or board with a common simultaneous clock. This buffering delays the clock signal and therewith consequently introduces a phase error which is indicated by an undesired delay in the block. This undesired delay may vary in accordance with variations in the circuits used. In order to establish a given phase for the local clock, there is used a fixed additional delay which is larger than the undesired delay and after the undesired varying delay the phase for the local clock can be established in accordance with the function illustrated in Figure 2, with the aid of a phase comparator and a variable delay. Because the undesired delay can be compensated-out in this way, it is possible to work at a higher clocking frequency and to maintain synchronism to a better extent than would otherwise be possible.

Figure 3 is a block schematic which illustrates an inventive device for phase locking onto a reference clock, wherein an undesired delay FD is compensated for at the same time. The inventive device permits a digitally continuous incrementally variable change in the delay and compensates the phase with, in principle, an unlimited number of steps. The device illustrated in Figure 3 includes a local clock pulse generator 2 in the form of a crystal oscillator XO whose output signal shall be compensated for the delay FD, for instance in a buffer arrangement 3, it being desired that the phase of the local clock will coincide with an external reference 1. The external reference 1 is

considered to have the same frequency as the local crystal oscillator XO. A phase comparison with the outer reference is effected conventionally with the aid of a phase comparator 5 which steers a control logic 4. The control logic includes a conventional up-and-down counter which steers two variable delay lines 10 and 11 which are parallel connected in series with the local clock pulse generator 2. In turn, each delay line 10 and 11 includes a finite number of small delay elements, wherein a delay is obtained by digitally controlling the circuit so that the signal will be taken out after having passed a given number of such incremental delay steps. The circuit also includes a selection circuit which is controlled by control logic to select the signal from either of the variable delay lines 10 and 11 and to deliver the signal to the buffer arrangement 3 which implements the delay FD, which is not fully known and may possibly vary. The outputs from the two variable delay lines 10 and 11 are also delivered to a further phase comparator 7 which operates in principle in the same manner as the phase comparator 5. In the case of the illustrated, preferred embodiment, the control logic operates with the assumption that the phase comparator 7 of this exemplifying embodiment is supplied on its inputs with signals that have an absolute phase difference  $2N\pi$ , where n is a positive or a negative integer other than zero. In the preferred, exemplifying embodiment  $N = -1$  or  $+1$ , which is the most favourable value with regard to the delay line. In turn, the phase comparator 7 delivers a control signal to the control logic 4.

The device illustrated in Figure 3 operates in the following manner. The variable digital delay lines 10 and 11 are stepped through the control logic in response to the control signal from the phase comparator in a known manner, so that the signal phase delivered by both the variable delay line 10 and the variable delay line 11 will each compensate for the delay FD in the buffer arrangement 3 so that the phase of the local clock will coincide with the external reference 1. In this regard, the counters of the control logic will steer the variable delay lines 10 and 11 so that one delay line will lie within a first half of its full

delay interval, while the other delay line will lie correspondingly in another half of its full delay interval, i.e. there will be a difference of, for instance, precisely  $2\pi$  in absolute phase between their outputs which supply the selection circuit 6.

The control logic 4 causes the selection circuit to choose one input signal which in this case is then sent to the buffer arrangement 3. Phase errors between the signal from the crystal oscillator 2 and the external reference will be compensated for continuously and constantly in small discrete steps. Should the active delay circuit delivering the signal distributed by the selection circuit 6 to the buffer arrangement 3 begin to approach its phase compensation limit, the control logic will conventionally order the selection circuit to switch-over and instead allow the signal from the other delay line to pass through, this other delay line hitherto being the inactive signal transducer. The changeover between these variable delay lines occurs momentarily on the local clock since, in principle, they have the same relative phase and since the absolute phase in the illustrative preferred embodiment differs between the two delay lines 10 and 11 by precisely  $2\pi$ .

Consequently, such a command from the control logic 4 to the selection circuit will result in the earlier active variable delay line becoming passive and the earlier passive circuit becoming active. If the phase drift then continues so as to pass the delay regulation limit of the now passive circuit, the control logic resets the counter value thereof so that it will jump  $2\pi$  forwards or backwards in phase. This phase jump, however, will not affect the phase of the local clock, which is continuously supplied via the active delay line. Upon completion of the phase jump of  $2\pi$ , the relative phase of the passive delay line can again be obtained equal to the phase of the active delay line, with the aid of the phase comparator 7 and the control logic. Thus, there is now no critical time period in which to achieve this phase realignment. By constantly switching between the variable delays 10 and 11 in the described manner and then

adjusting the inactive delay line, it is possible to adjust the delay with an unlimited number of unit steps without progressing beyond the phase adjustment range and without the outgoing signal phase being involved in the otherwise necessary phase jump  $N \times 2\pi$ , where  $N$  is a positive or a negative integer.

Figure 4 illustrates a further embodiment according to the present invention, comprising a device which instead of two separate, variable delay lines 10, 11 uses one single digital delay line 15 which includes a double array of signal tapping points or outlets. Remaining blocks 1-7 correspond to similar functional blocks in Figure 3. Each signal outlet in the delay line is selected digitally by two control inputs which are controlled by the control logic 4, similar to the Figure 3 embodiment. Thus, in this case, the actual delay line 15 is constantly active and instead operates with an active and an inactive signal tapping of the delay line. In other respects, the function is identical with the function discussed with reference to Figure 3. This latter solution, however, has the advantage that any differences in manufacturing tolerances with regard to the delay steps in separate delay lines such as lines 10 and 11 in Figure 3 will be avoided by the solution according to Figure 4.

Figure 5 illustrates a use application of the clock oscillator arrangement in accordance with the present invention. In the illustrated case, the device represented by the block schematic in Figure 5 operates with three different planes referenced A, B and C, each of which includes a respective crystal-controlled clock oscillator XO, although the arrangement may, of course, be expanded with further planes. A reference or master is selected via a respective selector SA, SB and SC with the aid of maintenance logic ML1, ML2 and ML3 respectively, each of which influences the choice of reference at selector SA, SB and SC with a respective control line M1, M2 and M3. According to the invention, each oscillator XO is controlled and phase-compensated against the selected reference in accordance with Figure 3 or

Figure 4. Respective control logic CLA, CLB and CLC deliver an error indication signal CLERR to respective maintenance logic ML1, ML2 and ML3. In principle, this error indication signal is obtained with the aid of the phase comparator 5 in Figure 4 or Figure 5. The error indication signal indicates that a given plane is no longer able to align the phase of its crystal oscillator XO with a given reference phase. This thus indicates the existence of an error, but because the redundancy existing in the system the faulty oscillator can be excluded from the system until the error has been rectified. The total function of the system will therefore not be affected. The inventive circuit thus enables the phase output of each plane to be monitored and controlled continuously, so that this phase will coincide with the phase of the other two planes in normal cases when no error or fault exists. It will be seen that, in principle, any one of planes A, B or C can serve as a reference and that if one plane should become faulty, there still remain two planes which, in principle, can control each other until the faulty oscillator XO has been rectified.

## CLAIMS

1. A method for aligning the phase of a stable local frequency oscillator (2) whose phase and frequency differ from an internal or external reference (1), by utilizing a phase comparator (5) and a digitally incrementally variable delay line so as to align the phase of the signal from the stable local frequency oscillator with the internal or external reference frequency phase (1), characterized by

switching between an active delay line (10, 11) and an inactive delay line (11, 10) in series with the signal from the oscillator (2) when the active delay line approaches its phase adjustment limit, there being in absolute phase a difference of precisely one whole clock period or several whole clock periods between the active and the inactive delay line, wherein when switching between said lines there is achieved an exchange of function such that the earlier active delay line will then constitute the inactive delay line and the earlier inactive delay line will constitute the active delay line up to the time at which a further switch is made, so as to obtain delay-wise unlimited continuous incremental phase alignment of the signal from the local oscillator (2) with the internal or external reference phase (1); and by

adjusting the inactive delay line with at least plus or minus one clock period of said oscillator (2) when said inactive delay line approaches the limit of its phase regulating ability, such that the relative phase from said inactive delay line will continue to coincide with the output phase from the active delay line.

2. The method according to Claim 1, characterized by using two distinct parallel incrementally variable delay lines (10, 11) whose mutually relative delays differ by a value which corresponds at least to one whole period at the frequency of the oscillator (2).

3. The method according to Claim 1, characterized by using an

incrementally variable delay line (15) which includes two arrays of tapping-points whose mutually relative delays differ by an amount which at least corresponds to one whole period of the frequency of the oscillator (2).

4. A device for aligning the phase of the signal from a stable local frequency oscillator with the phase of a given reference frequency, comprising a phase comparator (5), counter logic and a digitally incrementally-variable delay line, characterized in that the device further includes an additional phase comparator (7) and a selection circuit (6), said selection circuit being controlled by control logic (4) including the counter logic;

that the variable delay line in series with the oscillator (2) is parallel-divided into a first delay line and a second delay line which, with the aid of the additional phase comparator (7) produce the same relative phase delay, wherein the first delay line is placed in an active mode by the selection circuit whereas the second delay line becomes inactive and the inactive delay line obtains an absolute phase which differs by plus or minus one full period or several full periods of the oscillating frequency of the oscillator (2); and

that the selection circuit delivers the signal from the delay line that has been placed in an active mode.

5. The device according to Claim 4, characterized in that the first and the second variable delay lines comprise two distinct and mutually separate incrementally variable delay lines (10, 11).

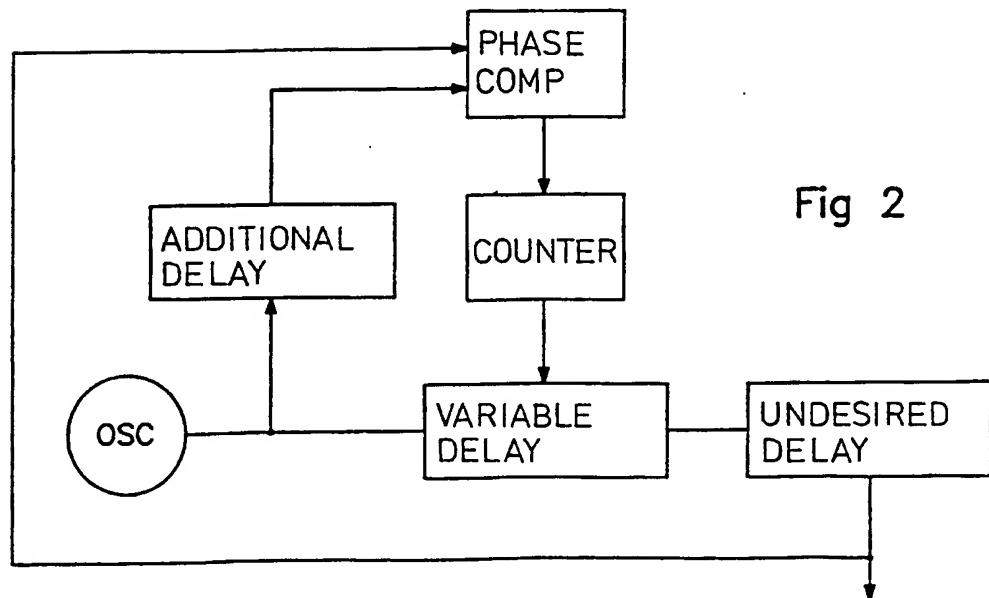
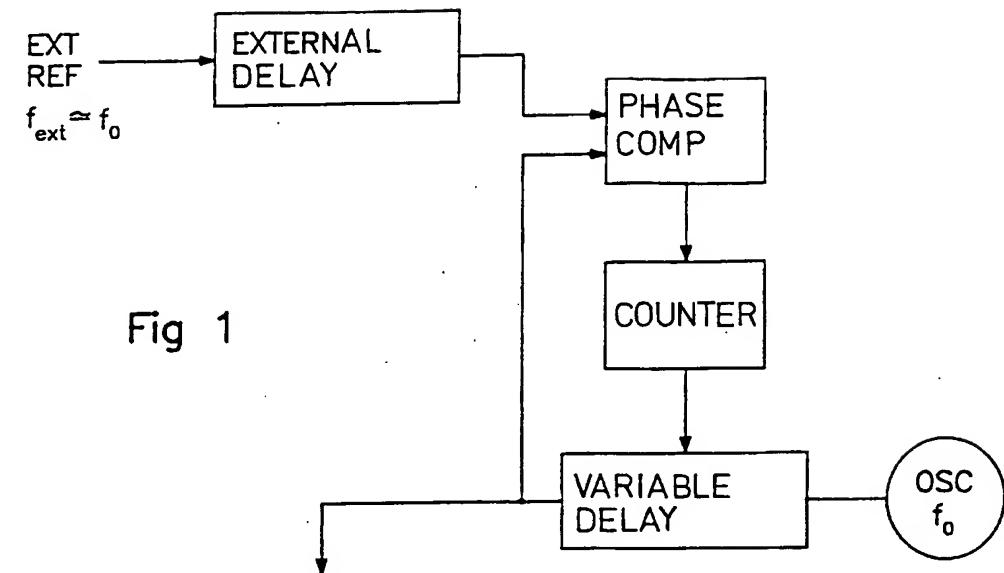
6. The device according to Claim 4, characterized in that the first and the second variable delay lines are comprised of one single incrementally variable delay line (15) which includes two mutually separate and controllable tapping-points.

7. The device according to Claim 5 or 6, characterized in that the device with the exclusion of a resonator element for the

oscillator (2), preferably a quartz crystal, forms an integrated circuit module.

8. The device according to Claim 5 or 6, characterized in that the device inclusive of a resonator element, preferably a quartz crystal, for the oscillator (2) forms an LSI-module.

WO 94/26032



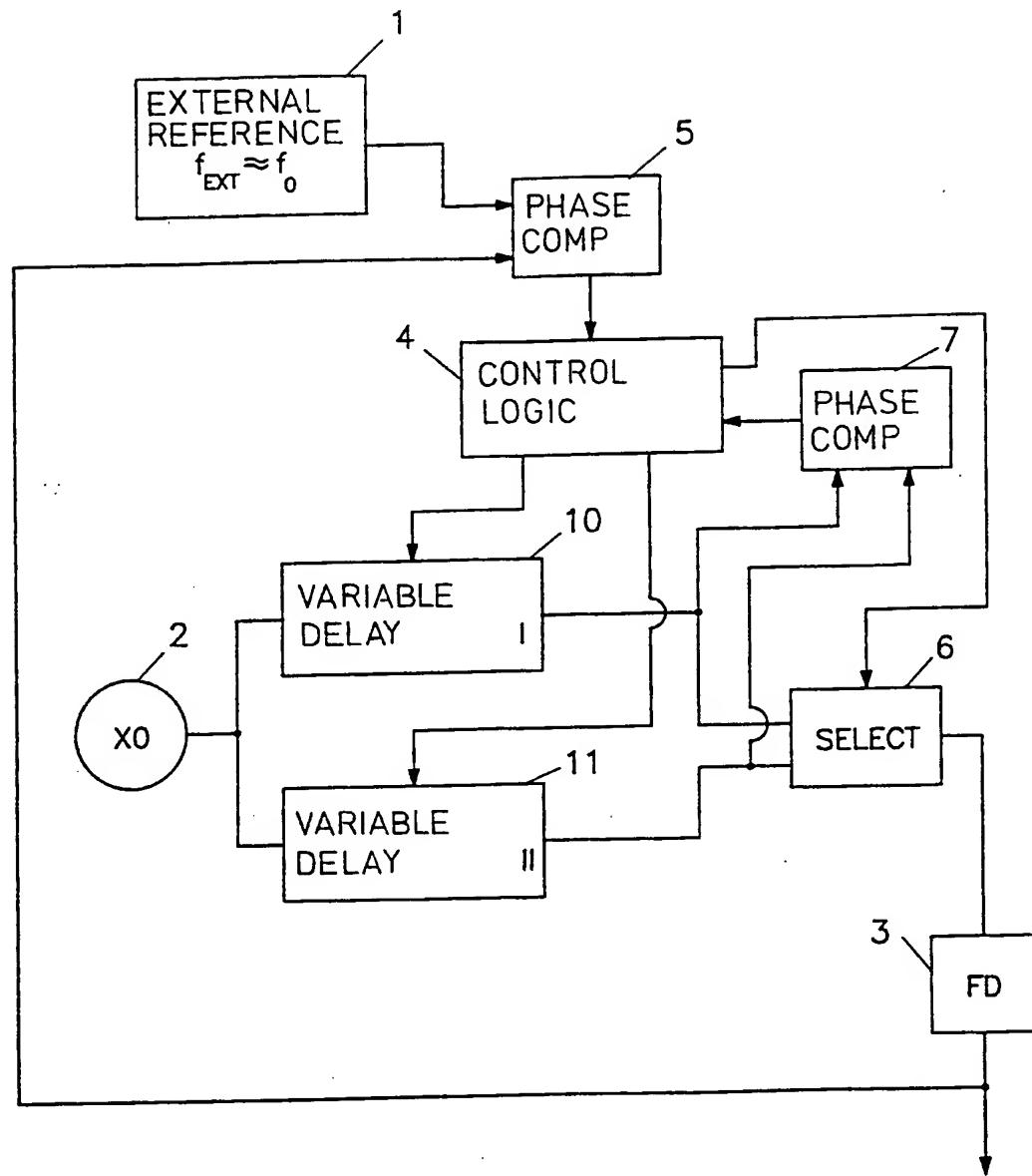


Fig 3

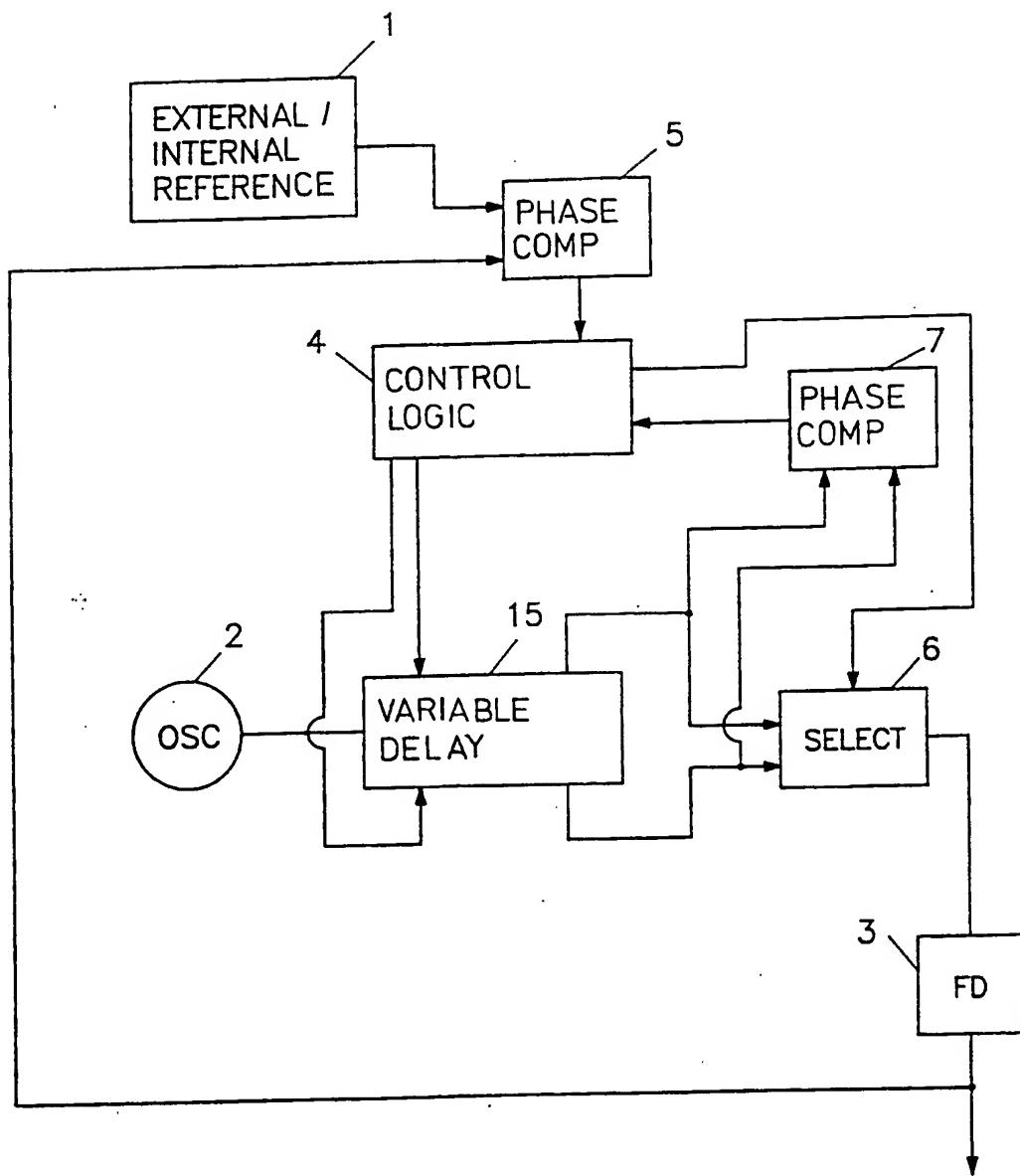


Fig 4

WO 94/26032

## BACK PLANE

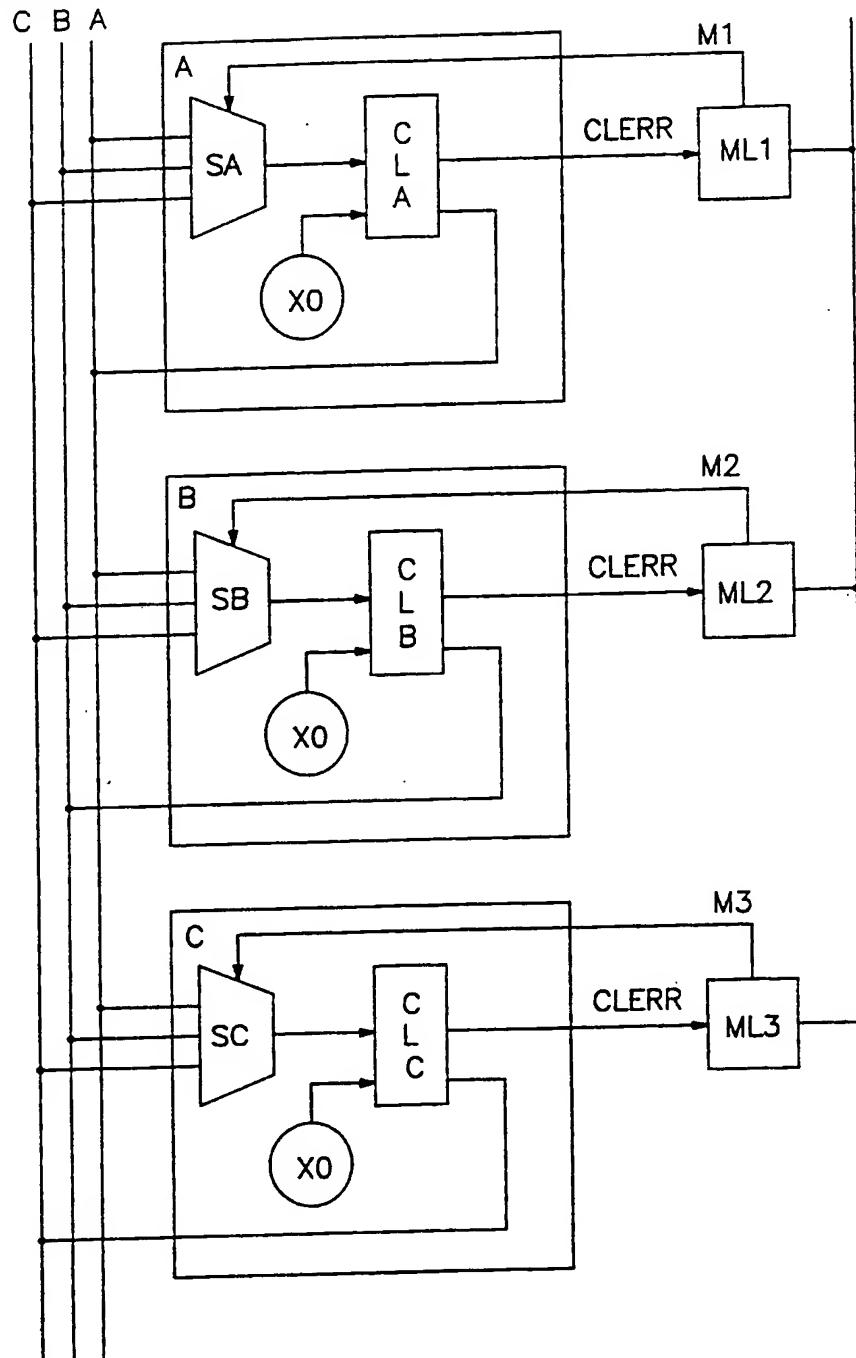


Fig 5

## INTERNATIONAL SEARCH REPORT

1

International application No.  
PCT/SE 94/00268

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
IPC5: H03L 7/081, H04L 7/033 According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols)		
IPC5: H03L, H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
SE, DK, FI, NO classes as above		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used).		
<b>CLAIMS, WPI, INSPEC, JAPIO</b>		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5079519 (LAURIN ASHBY, ET AL), 7 January 1992 (07.01.92), column 4, line 10 - line 51; column 15, line 39 - column 20, line 11, cited in the application  --	1-8
A	US, A, 4677648 (ERWIN A. ZURFLUH), 30 June 1987 (30.06.87), column 2, line 38 - line 66; column 7, line 15 - column 8, line 21, cited in the application  --	1-8
A	US, A, 4868514 (MICHAEL J. AZEVEDO ET AL), 19 Sept 1989 (19.09.89), column 1, line 65 - column 2, line 44, cited in the application  --	1-8
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "B" earlier document but published on or after the international filing date "C" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "D" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
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## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4795985 (SAMUEL H. GAILBREATH, JR.), 3 January 1989 (03.01.89), abstract, cited in the application ---	1-8
A	GB, A, 2236223 (OKI ELECTRIC INDUSTRY CO LTD), 27 March 1991 (27.03.91), page 5, line 18 - page 7, line 14, cited in the application -----	1-8

**INTERNATIONAL SEARCH REPORT**  
Information on patent family members

02/07/94

International application No.	
PCT/SE 94/00268	

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 5079519	07/01/92	NONE		
US-A- 4677648	30/06/87	EP-A,B-	0185779	02/07/86
US-A- 4868514	19/09/89	DE-D- EP-A,B-	3889525 0318155	00/00/00 31/05/89
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